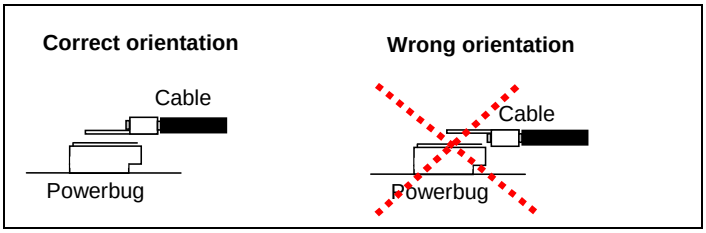
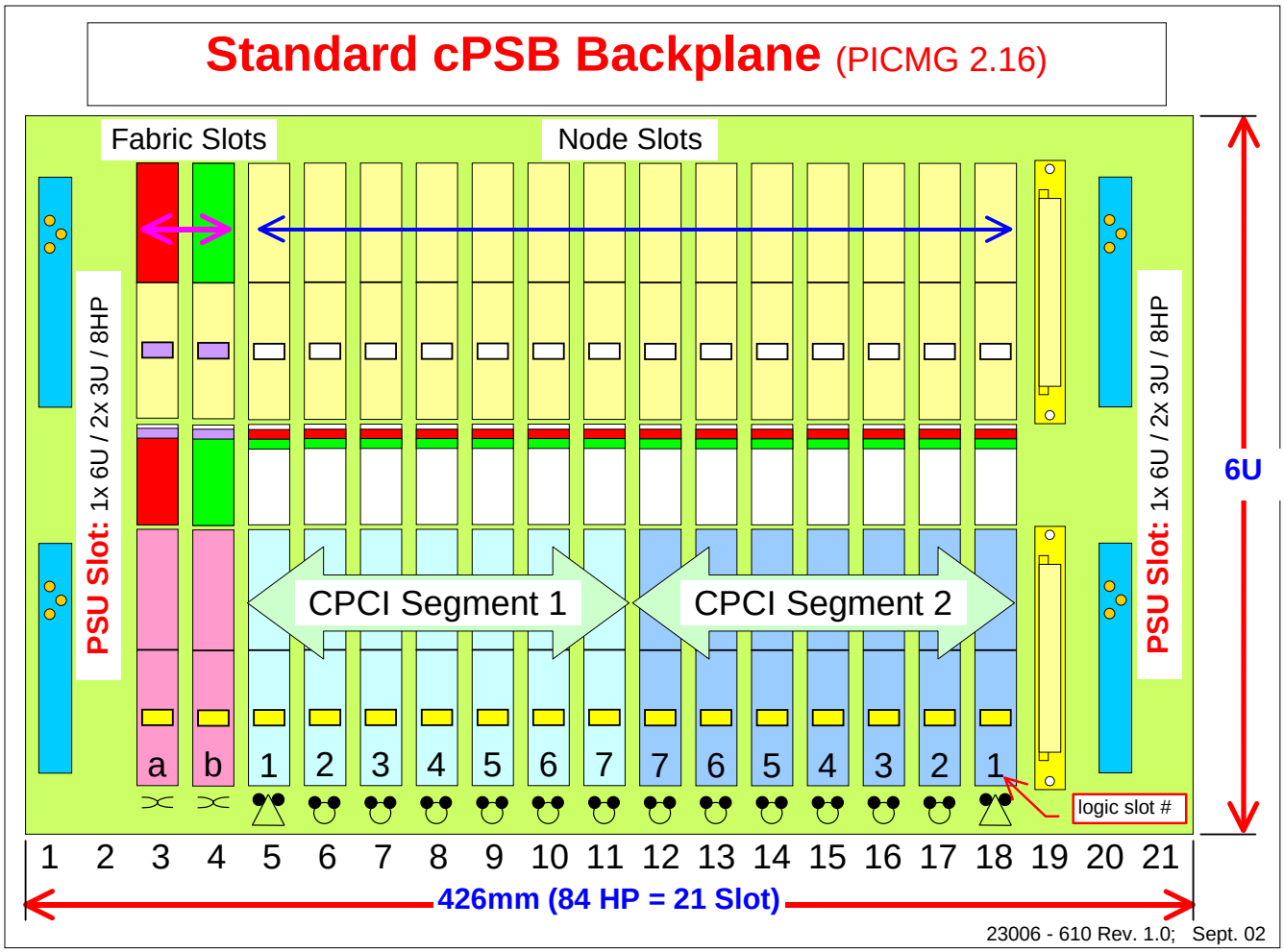
Assembly Instructions & general Information

1. **Mechanical Mounting:** Attach the backplane through the mounting holes in at least every second connector position at top and bottom using M2,5 screws and isolating washers.
2. **Chassis GND:** If noise reduction shall be achieved by connecting digital GND to Chassis GND, use conductive washers instead of isolating ones. Spring washers are recommended instead of flat washers. Creepage and clearance between screw and GND are in accordance with EN60950 is maintained by layout when using isolating washers.
3. **VI/O:** Check VI/O coding and VI/O (power) bridge, default assembly is +5V (blue key at connector P1). If VI/O shall be set to 3,3V, use conversion kit (order# 21101-658, including keys and tool) to change keys and move the bridge on rear. For position of the bridge see drawing #1.
4. **Geographical Addressing** (GA) is set by default to start from number one from left upper position within the chassis. If more than one backplane shall be assembled, a change of geographical addresses can be made. Cut copper links in between SMD pads to open, and zero Ohm resistors to close. Package size shall be 0603. Position is labelled "nGA[x]" where "n" stands for slot# , and "x" for address#, see drawing #1.
5. **M66MHz Operation:** Schroff CPCI backplanes are designed in accordance with the requirements of CPCI Core Specification, Revision 3.0 (PICMG 2.0 R3.0). Up to 5 Slots 66MHz operation is possible, signal M66 is HIGH (open). Backplanes of higher slot count also fulfil the 66MHz operation requirements in terms of clock trace length and skew, but M66 is tied to GND to disable 66MHz operation by default. This link is made by a removable copper link. For test purposes it can be opened and closed again by using a zero Ohm resistor of size 0603. For position of the link see drawing #1.
6. **Hot Swap:** Schroff CPCI backplanes fulfil the requirements for Basic Hot Swap of the Hot Swap Specification PICMG 2.1 R2.0. The signal BD_SEL# is tied to GND by a removable copper link. It can be replaced by a resistor-capacitor combination, both of package size 0603. Position is labelled "nB" where "n" stands for slot# , see drawing #1.
7. **Dimensions** 6U, 84HP
8. **Assembling of Power Cables:** M4 cable lugs should be used to connect the cables from the PSU to the powerbugs on the backplane. Maximum 2 cables are recommended per powerbug. Please assemble the cable lugs with the flat side to the power bug to ensure the correct isolation distance between unisolated part of the power cable and unisolated parts of the backplane.

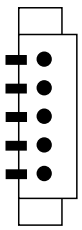


9. **CPSB Bus**
   - 2 Fabric Slots including optional Link between both
   - 14 Node Slots
   - redundant Chassis Monitoring Slots (IPMI Alarm module), hot swappable
   - 2 PSU Slots acc. to PICMG 2.11 (2x 6U PSU's or 4x 3U PSU's on top of each other)
     PSU slots placed at both ends of the Backplane
   - Fabric Slots are placed left of the Node Slots
   - CompactPCI bus (PICMG2.0 R.3.0) is implemented at Node Slots; two independent segments of System Slot left and right
   - Computer Telephony Bus (H.110) is not implemented on the P4 area, but can be easily implemented for custom purposes
   - Applicable Specifications:
     - PICMG 2.16 R1.0 Packed Switched Backplane
     - PICMG 2.0 R3.0 CPCI Core Specification
     - PICMG 2.01 R2.0 Hot Swap
     - PICMG 2.09 R1.0 System Management Bus
     - PICMG 2.10 R1.0 Keying
     - PICMG 2.11 R1.0 Power Interface Specification



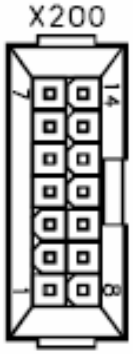
PICMG 2.16 Backplane Topology

IPMB Connectors (X101, X102, X103)



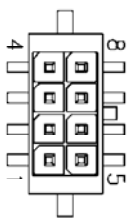
Pin	X101 (IPMB_0)	X102 (IPMB_1)	X103 (IPMB_2)
1	IPMB_SCL	IPMB_SCL_1	IPMB_SCL_2
2	GND	GND	GND
3	IPMB_SDA	IPMB_SDA_1	IPMB_SDA_2
4	IPMB_PWR	IPMB_PWR	IPMB_PWR
5	SMB_Alert	SMB_Alert	SMB_Alert
S1	GND	GND	GND
S2	GND	GND	GND

FCM (X200)



Pin	Signal
1	+12V
2	+12V (LED)
3	+3,3V (LED)
4	TEMP_Fail
5	TEMP_Fail_GND
6	FAN_Fail
7	FAN_Fail_GND
8	-12V
9	-12V (LED)
10	+5V
11	GND
12	Cmm_Bus_SDA
13	Cmm_Bus_SCL
14	Cmm_Bus_GND

AC-Fail (X190)



Pin	Signal
1	Input1_Fail
2	Input2_Fail
3	nc
4	INH#
5	GND
6	GND
7	nc
8	GND

SMD Switches (S101, S102, S103) (Signal to GND)

Pin	S101	S102	S103
1	SGA0_A	SGA0_B	CA_A0
2	SGA1_A	SGA1_B	CA_A1
3	SGA2_A	SGA2_B	CA_A2
4	SGA3_A	SGA3_B	CA_A3
5	SGA4_A	SGA4_B	CA_A4
6	nc	nc	nc

P47 connectors (X110, X120, X130, X140)

Pin#	Signal Name	Pin#	Signal Name
1	+5V	25	GA0
2	+5V	26	RESERVED
3	+5V	27	GND (EN#)
4	+5V	28	GA1
5	GND	29	nc
5	GND	30	+5V (V1 SENSE)
7	GND	31	GA2
8	GND	32	nc
9	GND	33	+3,3V (V2 SENSE)
10	GND	34	GND (GND Return)
11	GND	35	V1 SHARE
12	GND	36	+12V (V3 SENSE)
13	+3,3V	37	IPMB_SCL
14	+3,3V	38	PSU (1-4) DEG#
15	+3,3V	39	INH#
16	+3,3V	40	IPMB_SDA
17	+3,3V	41	V2 SHARE
18	+3,3V	42	PSU (1-4) FAL#
19	GND	43	IPMB_PWR
20	+12V	44	V3 SHARE
21	-12V	45	PE
22	GND (Signal return)	46	AC Input neutral
23	nc	47	AC Input line
24	GND		

Geographical Addressing

	X110	X120	X130	X140
GA0	GND	open	GND	open
GA1	GND	GND	open	open
GA2	GND	GND	GND	GND

CMM Master (X210, X220)

Reihe a		Reihe b		Reihe c	
1	+5V	1	+5V	1	+5V
2	+12V Sense	2	nc	2	PSU1_FAL#
3	+5V Sense	3	nc	3	PSU2_FAL#
4	+3,3V Sense	4	nc	4	PSU3_FAL#
5	-12V Sense	5	nc	5	PSU4_FAL#
6	nc	6	nc	6	PSU1_DEG#
7	nc	7	nc	7	PSU2_DEG#
8	GND	8	nc	8	PSU3_DEG#
9	Sysfail	9	nc	9	PSU4_DEG#
10	FAL#	10	nc	10	GND
11	DEG#	11	nc	11	Input1_fail
12	GND	12	nc	12	input2_fail
13	nc	13	nc	13	GND
14	nc	14	nc	14	GND
15	nc	15	nc	15	CA_A0
16	nc	16	nc	16	CA_A1
17	nc	17	nc	17	CA_A2
18	nc	18	nc	18	CA_A3
19	nc	19	nc	19	CA_A4
20	nc	20	nc	20	GND
21	GND	21	nc	21	Cmm_Bus_SDA
22	nc	22	nc	22	Cmm_Bus_SCL
23	nc	23	nc	23	Cmm_Bus_GND
24	nc	24	nc	24	nc
25	nc	25	nc	25	nc
26	GND	26	nc	26	GND
27	nc	27	nc	27	nc
28	nc	28	nc	28	nc
29	GND	29	nc	29	GND
30	nc	30	nc	30	nc
31	nc	31	GND	31	nc
32	GND	32	GND	32	GND